Am ndments to the Sp cification:

Please replace the third full paragraph on page 7 (lines 26-31) and continuing to the first partial paragraph of page 8 (lines 1-7) with the following paragraph:

FIG. 4A illustrates a cross section of a portion of the printhead 100 of FIG. 1 in one embodiment, for illustrative purposes only. FIG. 4B is a block diagram showing the embodiment of FIG. 4A. The layers of FIG. 4A and 4B are presented as an illustration and are not to scale. Referring to FIG. 1 and FIG. 2 along with FIGS. 4A and 4B, in one embodiment, the primitives 1-n 108, 110 are made of thin films and include an orifice plate 315 with nozzles 318 mounted on a barrier 375 that is coupled to a thin film circuit 401. Also included is a metal stack 403 comprised of a first metal layer 402 and a second metal layer 404. The first metal layer 402 can be Aluminum Copper Silicon. The second metal layer 404 includes plural power vias 406 (FIG. 4A illustrates one power via 406 and one resistor 112 for illustrative purposes only) and includes a top conductive metal 400~~, which can be Aluminum,~~ and a bottom metal barrier 407, which can be Tantalum Aluminum. ~~Resistor 112 is defined by a portion of the top conductive metal 400 and the bottom metal barrier 407.~~ The separation barrier 408 is defined by a bottom portion of the power via 406 that is adjacent to the first metal layer 402. Also, other layers 411 of FIG. 4A are included, but are not described here for simplicity.

Please replace the second full paragraph on page 8 (lines 8-17) with the following paragraphs:

The power vias 406 form an interface between the first metal layer 402 and the second metal layer 404 for providing power and control to the resistors 112. Also, the power vias 406 form a blockade between the second metal layer 404 and a substrate 409. The substrate 409 could be tetraethylorthosilicate (TEOS) or some such other compound. The separation barriers 408 of the respective power vias 406 are formed between conductive portions of the thin film resistor 112 and an associated power source 430, similar to power source 130 of FIG. 1, which derives power from the power bus 128 of FIG. 1. The separation barrier 408 is preferably made of a non-corrosive material, such as Tantalum Aluminum, Tungsten Silicon Nitride, or Tantalum Nitride. As a result, the electrical properties of the circuit are minimally affected while decreasing the possibility of

an electrical open.

As shown in FIGS. 4A and 4B, power via 406 defines a connection or interface between the top conductive metal layer 400 and the bottom of metal barrier layer 407. Some of the power vias 406 can form the separation barrier 408 between the resistors 112 and the first metal layer 402 to create a barrier between the resistors 112 and the power bus 128 of FIG.1 of the power source 430. In one embodiment, the top conductive metal layer 400 layer can be deposited on top of the bottom of metal barrier layer 407 for connecting the top conductive metal layer 400 to the bottom of metal barrier layer 407 through the holes or vias. The power via 406 can be created by standard thin film fabrication techniques, such as by using masking and etching steps to create holes that are formed at strategic points in the thin film circuit 401.